REMARKS

Claims 20-40 were pending in the present application. Claims 21 and 34 have been cancelled. Claims 41 - 42 have been added. Accordingly, claims 20, 22-33, and 35-42 are now pending in the application.

Claim 1 is objected to for informalities. Applicant assumes that the Examiner is referring to claim 20. Claim 20 has been amended accordingly.

Claims 22 and 35 stand rejected under 35 U.S.C. §112, 1st paragraph as failing to comply with the written description requirement. Applicant has amended claims 22 and 35 and believes the rejection to now be moot.

Claims 20, 23-33, and 36-40 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Schmidt (U.S. Patent No. 7,142,882) in view of Applicant Admitted Prior Art. Although Applicant respectfully traverses at least portions of this rejection, Applicant has amended the claims and believes the rejection to now be moot.

Claims 21-22, and 34-35 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Schmidt in view of Stravers (WO 03/005225). Although Applicant respectfully traverses portions of this rejection. Applicant has amended the claims and believes the rejection to now be moot.

Support for the amendments may be found throughout the specification, but specifically at, for example, page 2, lines 1-7; page 7, lines 13-18, the Abstract, and the original claims.

Applicant's claim 20 recites a wireless communication device comprising:

> a single integrated circuit die including:
> a reconfigurable processor core including a plurality of processors,
> wherein a first portion of the plurality of processors is configured
> to execute instructions belonging to an instruction set of a first

processor family and wherein a second portion of the plurality of processors is configured to execute instructions belonging to an instruction set of a second processor family, wherein the second portion of the plurality of processors is coupled to memory locations storing instructions executable by the second portion to implement a set of host processor functionality that includes controlling portions of the reconfigurable processor core and interfacing with a system external to the wireless communication device;

a non-reconfigurable host processor coupled to the reconfigurable processor core and configured to execute instructions belonging to an instruction set of a first processor family, wherein the non-reconfigurable host processor is coupled to memory locations storing instructions executable by the non-reconfigurable host processor to implement the set of host processor functionality; and

a processor type select circuit configured to select either the non-reconfigurable host processor or the second portion of the plurality of processors to implement the set of host processor functionality. (Emphasis added)

The Examiner asserts Schmidt teaches all of the limitations recited in claim 20, with the exception of the recited "processor" being a host processor, which the Examiner asserts is taught in the AAPA. As described in the previous response to Office action, dated January 17, 2008, Applicant submits the following paragraph is not found in Schmidt and is found in the specification of Applicant's instant application,

> Moreover, a portion of the reconfigurable processor core **150** can be organized as a second host processor processing instructions belonging to a second host processor family, while the host processor **148** belongs to a first processor family that processes instructions belonging to the first host processor family instruction set. In one embodiment, the host processor **148** is MIPS compatible, while the second host processor portion of the processor core **150** can be ARM compatible.

See page 7, lines 13-18.

While Applicant does not claim to have invented the concept of a "host processor," Applicant submits that neither the background section (the AAPA, according to the Examiner) nor Schmidt teaches or suggests having a "non-reconfigurable host processor" execute instructions from a first instruction set and a second portion of the processors of the reconfigurable core that executes instructions that perform the

functionality of the host processor (i.e., "controlling portions of the reconfigurable processor core and interfacing with a system external to the wireless communication device" as in claim 20) using a second (i.e., different) instruction set. Similarly, the cited references do not teach or suggest a processor type switch that selects either the host processor or the second portion of the reconfigurable processor core to "implement the host processor functionality," as recited in claim 20.

In addition, claim 20 recites that the host processor is "non-reconfigurable" and is coupled to the reconfigurable core. As such, the host processor cannot, by definition, be one of the processors within Schmidt's processor core 150, as suggested by the Examiner in the rejection of claim 20.

In regard to the rejection of claims 21-22, and 34-35, Applicant notes Stravers discloses a system in which a number of processors may have different instructions sets. For example, Stravers illustrates in FIG. 1, general processors in the ARM and MIPS family, as well as three DSP processors each having a different instruction set. However, the processors are enabled one at a time by an enable circuit 6, and the outputs of the processors are multiplexed such that only one output may be chosen at a time. The remaining non-used processors are deactivated:

> the processor cluster further comprising a selection unit for selectively activating one of the plurality of processors… (*See* page 1, lines 18-19) (Emphasis added)
>
> The processor cluster can be configured such that exactly one processor is activating and has a connection with the cache memory. (*See* page 1, lines 24-25) (Emphasis added)
>
> Only one of the processors 2a…2e, can be activated (i.e. connected to the cache memory). … The other processors are deactivated. (*See* page 5, lines 6-9) (Emphasis added)

Accordingly, Applicant submits none of the cited references teach or disclose the combination of features recited in Applicant's claim 20. Thus, Applicant submits claim

20 and its dependent claims patentably distinguish over the cited references for at least the reasons given above.

Applicant's claims 33, 40, and 43 include features that are similar to the features recited in claim 20. Accordingly, for at least the reasons given above, Applicant submits claims 33 and 40, along with their respective dependent claims patentably distinguish over the cited references.

CONCLUSION

Applicants submit the application is in condition for allowance, and an early notice to that effect is requested.

If any extension of time (under 37 C.F.R. § 1.136) is necessary to prevent the above-referenced application from becoming abandoned, Applicant hereby petitions for such extension.

The Commissioner is authorized to charge any fees that may be required, or credit any overpayment, to Meyertons, Hood, Kivlin, Kowert & Goetzel, P.C. Deposit Account No. 501505/6057-61200/SJC.

Respectfully submitted,

Date: June 16, 2008

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